IN THE CLAIMS:

Please REPLACE claims 1, 2, 9, 11-14 and 16 and ADD claim 17 in accordance with the following:

1. (ONCE AMENDED) An instruction processing device, comprising:

a storage circuit storing a combination of address mode information of a fetched instruction [with] and an instruction address of the fetched instruction;

a branch instruction control circuit controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction; and

a transfer circuit transferring the address mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed.

2. (ONCE AMENDED) The instruction processing device according to claim 1, wherein said branch instruction control circuit stores a combination of address mode information of a branch destination of the branch instruction [with] and an instruction address of the branch destination.

9. (ONCE AMENDED) An instruction processing device, comprising:

a storage circuit storing a combination of mode information of a fetched instruction [with] and an instruction address of the fetched instruction;

a branch instruction control circuit controlling a branch instruction using the mode information if the fetched instruction is the branch instruction; and

a transfer circuit transferring the mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed.

11. (ONCE AMENDED) An instruction processing device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system, comprising:

a storage circuit storing a plurality of combinations of mode information [obtained when] of an instruction [fetch request is issued, with] to be fetched and an instruction address [for each port] of the instruction, each combination related to each of the plurality of instruction fetch ports; and

a fetch circuit performing an instruction fetch based on mode information corresponding to a port to be used.

12. (ONCE AMENDED) An instruction processing method, comprising:

handling mode information of an information processing apparatus, which is to be determined when fetching each instruction, as a part of an instruction address;

fetching an instruction;

storing mode information of the fetched instruction as a part of an instruction address of the fetched instruction in each cycle of an instruction process for the fetched instruction; and

controlling the instruction process for the fetched instruction based on the stored mode information.

13. (ONCE AMENDED) An instruction processing device, comprising:

storage means for storing a combination of address mode information of a fetched instruction [with] and an instruction address of the fetched instruction;

branch instruction control means for controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction; and

transfer means for transferring the address mode information stored in the storage means to the branch instruction control means when the branch instruction is executed.

14. (ONCE AMENDED) An instruction processing device, comprising:

storage means for storing a combination of mode information of a fetched instruction [with] and an instruction address of the fetched instruction;

branch instruction control means for controlling a branch instruction using the mode information if the fetched instruction is the branch instruction; and

transfer means for transferring the mode information stored in the storage means to the branch instruction control means when the branch instruction is executed.

16. (ONCE AMENDED) An instruction processing device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system, comprising:

storage means for storing a plurality of combinations of mode information [obtained when] of an instruction [fetch request is issued, with] to be fetched and an instruction address [for each port] of the instruction, each combination related to each of the plurality of instruction fetch ports; and

fetch means for performing an instruction fetch based on mode information corresponding to a port to be used.

17. (NEW) An instruction processing device, comprising:

a storage circuit to store a combination of mode information and an instruction address for instructions to be fetched;

a branch instruction control circuit to control execution of a branch instruction using the mode information after one of the instructions to be fetched has been fetched as the branch instruction; and

a transfer circuit to transfer the mode information stored in said storage circuit to said branch instruction control circuit when the branch instruction is executed.

REMARKS

In the Office Action mailed November 18, 2003 the Examiner noted that claims 1-16 were pending; objected to the specification and drawings; rejected claims 1-3, 5, 6, 8-10 and 12-15 under 35 U.S.C. § 102(b); and rejected claims 4, 7, 11 and 16 under 35 U.S.C. § 103. In rejecting the claims, U.S. Patents 5,142,630 to Ishikawa; 4,881,170 to Morisada; and 5,963,721 to Shiell et al. (References A-C, respectively) were cited. Claims 1-17 remain in the case. The Examiner's rejections are traversed below.

The Invention

The present invention is directed a system and method for controlling execution of a branch instruction accompanied by a mode change in hardware. Combinations of mode information for an instruction to be fetched and an instruction address are stored with each combination related to one of a plurality of instruction fetch ports. As a result, it is possible to store address mode information sets (respectively indicating the address modes based on which the instructions are executed along the instruction execution pipeline) as parts of individual instruction addresses in every associated cycle or execution stage. Thus, the instruction processing device can operate correctly even under a situation in which an instruction fetch unit and an instruction execution pipeline operate asynchronously and instructions are fed to the pipeline based on branch prediction when necessary.

In addition, branch history is maintained containing both the instruction address with accompanying address mode information of a branch instruction and a branch destination address with accompanying mode information for each branch instruction. Branch prediction is